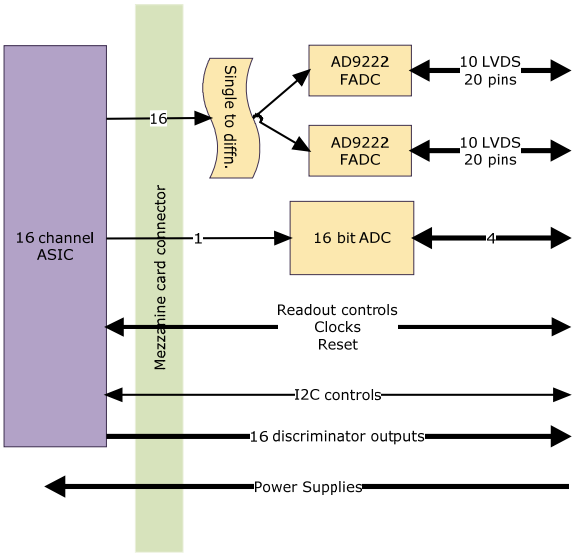
AIDA FEE specification

The FEE will interface the AIDA ASIC to the Data acquisition software, providing facility for control and event gathering. The ASIC will connect to the detector. Timing of events will be based on the BUTIS distributed clock. A signal will be provided for other parts of the experiment based on the OR of all the channel discriminators. Communication with the FEE for data transfer and control will be using an ethernet interface.

The FEE consists of a number of unit boards. Each board will contain sufficient equipment to support 8 ASICs and hence 128 detector channels. The unit will contain a number of FPGAs to carry out the tasks.



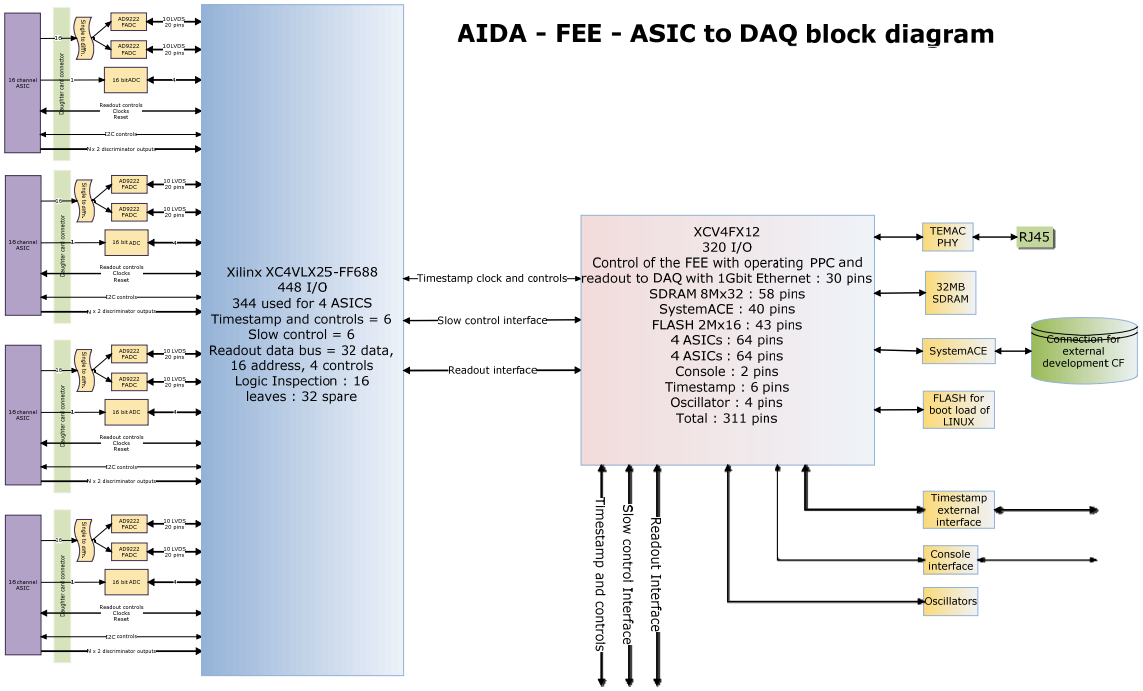
AIDA - FEE - Support connections and parts for one chip

Each ASIC requires the following interfaces and acquisition connections.

1. I^2C – bit serial register access route between the FEE and the ASIC. – 2 signals. Clock and bidirectional data.
2. Channel discriminator output to create timestamps of activity. – 16 logic signals.
3. Channel preamp outputs to create waveforms of activity detected by the discriminator. – 16 analogue signals with a single reference voltage.
4. Discriminator OR – True differential Logic signal to give 1ns timing. – 2 signals.
5. Multiplexed analogue – The output of the readout analog multiplexor. 1 signal with reference.
6. Readout information – Logic signals to indicate which channel is on the multiplexed analogue and allow handshaking between the ASIC control and the readout loic in the FPGA. 7 logic signals.
7. Readout control – Controls the output of multiplexed analogue. 4 signals including a RESET.

8. Calibration register control – Logic signals to control the calibration connections in the ASIC. A step voltage will inject the calibration charge to the selected channels. 3 Logic and one analogue.

The total number of connections to the ASIC required is 54.

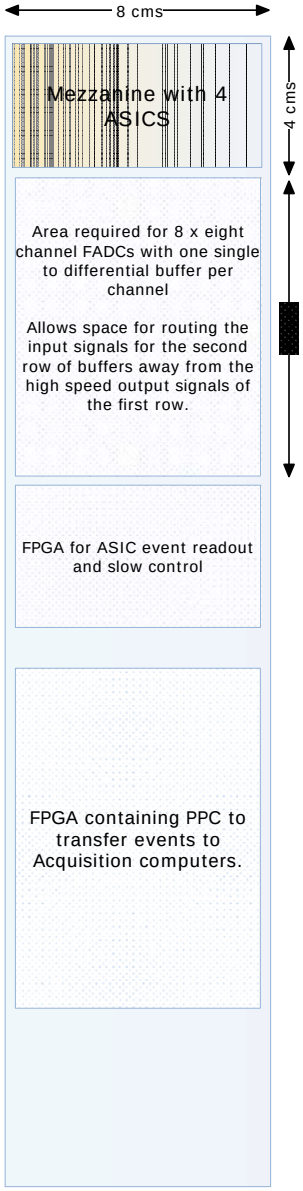


Constraints on the FEE.

The FEE must occupy boards with an 8cm maximum dimension at the interface with the detectors.
Each 8cm width must contain sufficient ASICs and acquisition electronics for 128 channels.

Proposed layout

The FEE for 128 channels will be split between two sub-boards. Each sub-board will contain the required electronics for 64 channels.
Each sub-board will connect to the Detector along half of it's 8cm length. The ASICs will be mounted on a mezzanine to allow for easy replacement in case of channel failure.
The sub-boards will connect to each other at the rear to allow a single FPGA containing a PPC to control the acquisition of data for all 128 channels. The two sub-boards will be identically designed at the front end and only differ in the rear area where the PPC FPGA resides.



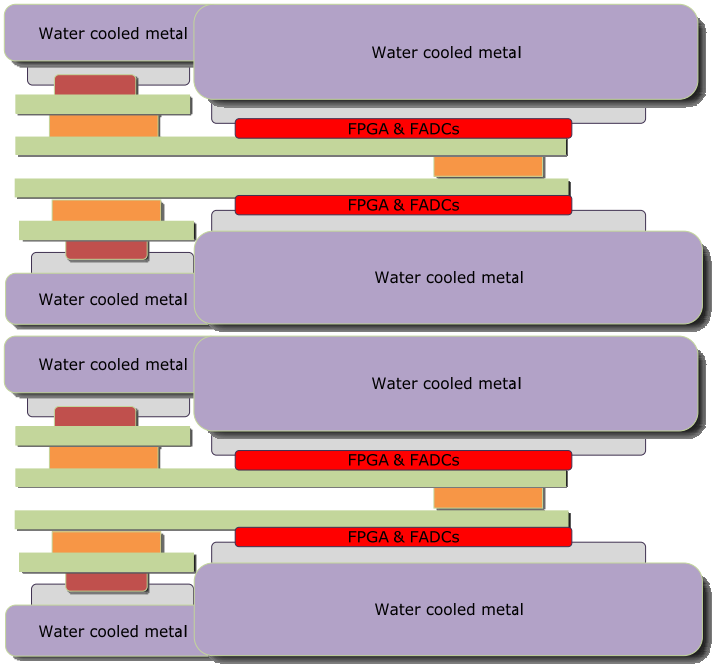


Diagram (above) of the FEE boards as they would fit in the vertical plane. The grey rectangles are heat conductive foam pads which conform to the component outlines and conduct the heat to the water cooled metalwork. The green is pcb, the orange is a Samtec 80 pin connector with a 2.3mm height and the dark brown is the ASIC. The connections to the detector will be on the mezzanine boards to the left and to the acquisition network computers and BUTIS on the right. These are not shown.

Diagram (alongside) shows the layout of a sub-board.

The stack height of the FEE boards for one detector is expected to be

4 x 1.6mm => 6.4 – FR4 pcbs
3 x 2.3mm => 6.9 – Samtec connectors
2 x 4mm => 8 – ASIC thickness
2 x 3mm => 6 – Heat conductive pad with compression (3.8mm)
=> 27.3mm.

Extra thickness will be required for the water cooled plates where they extend over the ASICs on the mezzanines. The mechanical structure of the FEE enclosure is not part of this specification at present.
Problems like how to install and remove the FEE when the ASICs are connected to the detector have not been resolved yet.

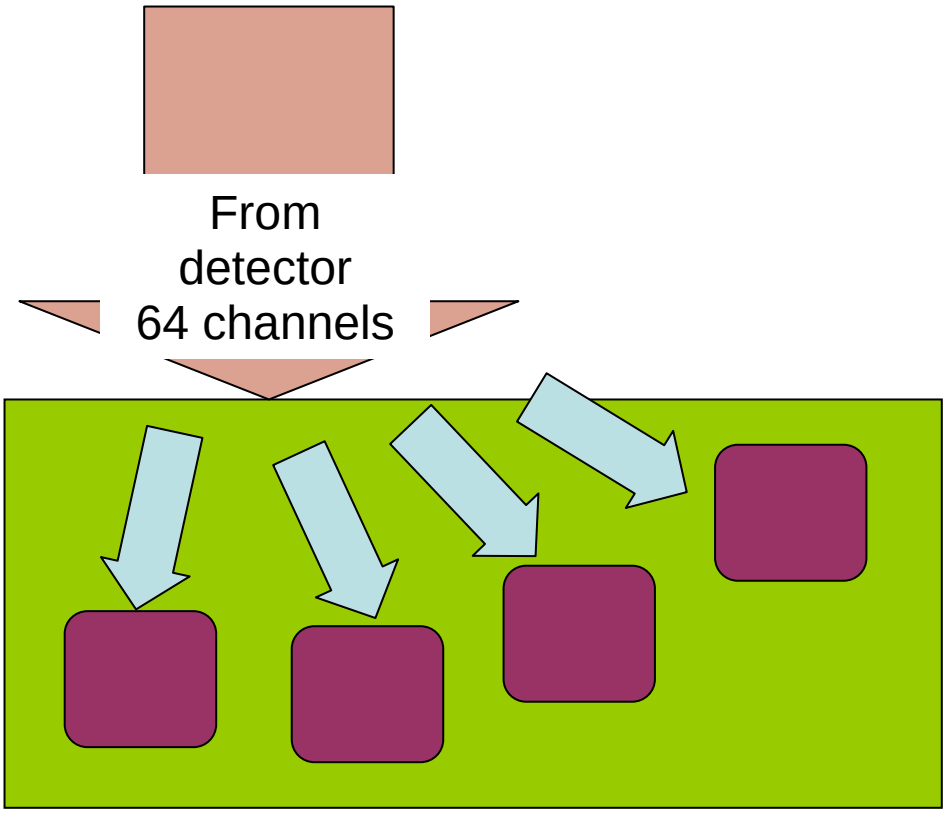


Diagram (above) illustrates the connection between the ASIC mezzanine and the detector.

The main components used.

One Xilinx Virtex4 FPGA will be used on each sub-board to control and collect events for four ASICs. One Xilinx Virtex4 will be used to collate the data and communicate with the Acquisition computers.

Each channel of fast analogue will be buffered using an AD8139 in CSP format which has a 3mm square footprint. Unfortunately each buffer requires eight discrete components and these are best mounted on the TOP side of the board to minimise vias.
Eight fast analogue channels will share one AD9222 flash ADC. Each device contains eight convertors with data readout from each convertor over seperate 300Mhz DDR serial links. The 300Mhz clock and a frame signal are provided for the FPGA to return the data to parallel form.

Each multiplexed analogue channel will be converted using an AD7686 (or equivalent) which is a small footprint serial output 500Ksps 16 bit ADC.